CLAIMS

1. A planar avalanche photodiode comprising:

an n-type semiconductor layer defining a contact area;

a semiconductor layer having a p-type diffusion region, the p-type diffusion region having a smaller area than the semiconductor layer;

a semiconductor multiplication layer;

a semiconductor absorption layer; and

a p-type contact layer;

wherein the p-type diffusion region is disposed directly adjacent to the p-type contact layer, and the semiconductor absorption layer is disposed between the semiconductor multiplication layer and the semiconductor layer with the p-type diffusion region.

2. The planar avalanche photodiode of claim 1 further comprising at least one grading layer disposed adjacent to the semiconductor absorption layer.

3. The planar avalanche photodiode of claim 1 further comprising a p-type semiconductor charge control layer disposed adjacent to the semiconductor multiplication layer.

4. The planar avalanche photodiode of claim 1 further comprising at least one n-type contact layer.

5. The planar avalanche photodiode of claim 1 wherein the n-type semiconductor layer is InAlAs.

6. The planar avalanche photodiode of claim 1 wherein the semiconductor layer with the p-type diffusion layer is InAlAs.

7. The planar avalanche photodiode of claim 1 wherein the semiconductor multiplication layer is InAlAs.

8. The planar avalanche photodiode of claim 1 wherein the semiconductor absorption layer is InGaAs.

9. A method of fabricating a planar avalanche photodiode comprising the following steps:

providing an n-type semiconductor layer defining a contact area;

depositing a semiconductor layer;

depositing a semiconductor multiplication layer;

depositing a semiconductor absorption layer;

depositing a p-type contact layer; and

diffusing a p-type diffusion region having a smaller area than the semiconductor layer directly adjacent to the p-type contact layer, thereby decreasing the capacitance of the planar avalanche photodiode.

10. The method of claim 9 further comprising the step of depositing at least one grading layer adjacent to the semiconductor absorption layer.

11. The method of claim 9 further comprising the step of depositing a p-type semiconductor charge control layer adjacent to the semiconductor multiplication layer.

12. The method of claim 9 further comprising the step of depositing at least one n-type contact layer.

13. The method of claim 9 wherein the n-type semiconductor layer is InAlAs.

14. The method of claim 9 wherein the deposited semiconductor layer is InAlAs.

15. The method of claim 9 wherein the semiconductor multiplication layer is InAlAs.

16. The method of claim 9 wherein the semiconductor absorption layer is InGaAs.

17. A planar avalanche photodiode including a n-type semiconductor layer defining a contact area and a p-type contact area, the planar avalanche photodiode comprising:

a semiconductor layer having a p-type diffusion region disposed directly adjacent to the p-type contact layer, the p-type diffusion region having an area smaller than the area of the semiconductor layer;

a semiconductor multiplication layer; and

a semiconductor absorption layer.

18. The planar avalanche photodiode of claim 17 wherein the n-type semiconductor layer is InAlAs, the semiconductor layer is InAlAs, the semiconductor multiplication layer is InAlAs, and the semiconductor absorption layer is InGaAs.

19. A planar avalanche photodiode comprising:

an n-type semiconductor layer defining a contact area;

a semiconductor multiplication layer;

a semiconductor absorption layer, the semiconductor multiplication layer being disposed between the first n-type semiconductor layer and the semiconductor absorption layer; and

a p-type semiconductor contact layer having a smaller area than the absorption layer, the semiconductor absorption layer being disposed between the semiconductor multiplication layer and the p-type semiconductor contact layer,

wherein the photodiode has a low field region near the p-type semiconductor contact layer and a low capacitance.

20. The planar avalanche photodiode of claim 19 further comprising at least one grading layer disposed adjacent to the semiconductor absorption layer.

21. The planar avalanche photodiode of claim 19 further comprising a p-type semiconductor charge control layer disposed adjacent to the semiconductor multiplication layer.

22. The planar avalanche photodiode of claim 19 wherein the n-type semiconductor layer is InAlAs.

23. The planar avalanche photodiode of claim 19 wherein the semiconductor multiplication layer is InAlAs.

24. The planar avalanche photodiode of claim 19 wherein the semiconductor absorption layer is InGaAs.

25. The planar avalanche photodiode of claim 19 wherein the p-type semiconductor contact layer is InAlAs.

26. The planar avalanche photodiode of the claim 19 further comprising a passivated region including a semiconductor layer disposed between the p-type contact layer and the semiconductor absorption layer.

27. The planar avalanche photodiode of claim 26 wherein the passivated region includes a portion of a first grading layer and a portion of the semiconductor absorption and multiplication layers.